**THAT WHICH IS CLAIMED IS:**

1. A digital electronic circuit providing high-level to low-level voltage translation with equal rise and fall delays and equal rise and fall transition times, comprising :

an input high-voltage logic inverter operating at the high-level voltage,

an output low-voltage logic inverter operating at the low-voltage level, and

a voltage translation means coupling the output of the high-voltage inverter to the input of the low-voltage inverter.

2. A digital electronic circuit as claimed in claim 1 wherein the voltage translation means is a digital electronic circuit comprising a plurality of series-connected transistors each of which is biased to provide a fixed voltage drop.

3. A digital electronic circuit as claimed in claim 2 wherein the voltage translation means provides a voltage that is not less than one threshold voltage below the low voltage level in the high state while ensuring that it never exceeds the maximum voltage rating of the low voltage transistors, so as to minimize output inverters leakage current and avoid the possibility of crowbar conduction or transistor breakdown.

4. A digital electronic circuit as claimed in claim 2 wherein the voltage translation means includes an additional transistor connected to feedback the output of the low-level inverter to its input to

minimize output leakage current and avoid the possibility of crowbar conduction.

5. A digital electronic circuit as claimed in claim 1 wherein the voltag translation circuit is a logic block that provides an output that follows the input until the low-voltage supply voltage iss reached and thereafter maintains the output at the supply voltage level while the input continues rising.

6. A digital electronic circuit as claimed in claim 5 wherein the logic block comprises a low-voltage transistor having its common terminal connected to the low-voltage supply while its output terminal is connected to, the output terminal of a transistor having its control terminal connected to the input of the voltage limiting circuit, while its common terminal provides the complementary output from the voltage limiting cirucit.

7. A method for translating a high-level voltage to a low-level voltage while providing equal rise and fall delays and equal rise and fall transition times comprising the steps of:

providing a high-voltage input inverter operating at the high-level voltage,

providing at the low-level voltage, and

coupling the output of the high voltage input inverter to the input of the low-voltage output inverter after degrading it to the required level.

8. A method as claimed in claim 7 wherein the degrading of the voltage level from the output of the high-voltage inputinverter is performed by passing it

through a plurality of transistors connected in series with each transistor being biased to provide a fixed voltage drug.

9. A method as claimed in claim 7 wherein the degraded voltage is adjusted to provide a voltage level that is greater than one threshold voltage below the low voltage level in the high state while ensuring that it never exceeds the maximum voltage rating of the low voltage transistors, so as to minimize output inverter leakage currect and avoid the possibility of crowbar conduction or transistor breakdown.

10. A method as claimed in claim 7 inlcuding providing feedback from the output of the output inverter to its input when the output is in the high state, so as to minimize output inverter leakage and avoid the possibility of crowbar conduction.

11. A method as claimed in claim 7 comprising the steps of:

limiting the output from the high-voltage digital inverter to the desired lower voltage levels; and

using the limited voltage swing to drive an output low-voltage digital inverter.

12. A method as claimed in claim 11 wherein the output from the high-voltage digital inverter is converted to the desired low voltage levels by voltage limiting it to the levels of the low voltage supply.